REMARKS

Applicant thanks the examiner for pointing out that claims 33-35 and 38-40 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 39 is amended to correct a typographical error. No claims are added or canceled.

Claims 31, 32, 36 and 37 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,991,014 (hereinafter "Takahashi") in view of U.S. Patent No. 5,416,529 (hereinafter "Lake"). Applicant respectfully disagrees.

The Office Action asserted that:

> "Lake also discloses the key processing unit loaded with array of key values (see column 5, lines 23-24) which in turn allows the office to interpret Lake to inherently load an array of key parameters (I_k, g_k, v and c_k) one for each pixel input."

Applicant respectfully submits that such an interpretation is incorrect. Column 5, lines 20-25, of Lake shows:

> "Key processor 13 of FIG. 2 is preferably an LUT which consists of hardware identical to the LUT hardware of key processor 3 of FIG. 1. However, processor 13 is loaded with an array of key values c_g, which are different from the values α loaded into processor 3 of FIG. 1."

It is very clear that what is loaded in the LUT is values c_g, not (I_k, g_k and c_k). From this description of Lake, one understands that processor 13 is preferably an LUT loaded with an array of values for the lookup of c_g, which is a function of I_k, g_k, v and c_k (see, e.g., equation 3 on Column 5 of Lake). The pixel value v is the input to the LUT from selector 1 (see, e.g.,

Figure 2 and lines 44-47 in Column 5 of Lake). The control parameters I_k, g_k and c_k are clip level, key gain and key insert respectively (see, e.g., lines 7-8 in Column 3 of Lake) which determine the values of c_g in the LUT. For a given set of control parameters, the values of c_g for the relative small number of discrete values v can be determined (e.g., using equation 3 of Lake) and loaded as the content of LUT. Once the values of c_g for different values of v are loaded into the LUT, a value v of a given pixel can be used as an input from selector 1 in Fig. 2 of Lake to look up the corresponding value c_g for the pixel.

A person skilled in the art understands that a look up table (LUT) is typically loaded with an array of values corresponding to different index values of an input. An input index to the look up table causes the look up table to look up a corresponding one of the array of values.

It is clear that what is loaded into the LUT of Lake ***before*** any look up operation is the array of values c_g corresponding to different values of v for one set of control parameters I_k, g_k and c_k. It is clear that I_k, g_k and c_k are ***not*** loaded into LUT. Further, I_k, g_k and c_k are ***not*** loaded into LUT *for each pixel.*

During a look up operation, a single pixel value v is use to look up a ***single*** corresponding value c_g. The value c_g is looked up one at a time for a pixel as a sequential scalar operation. There is no indication of vector processing in Lake.

Similarly, the assertion of "since Lake discloses producing a key signal for each input pixel and input parameter (I_k, g_k, v and c_k), the office interpretes Lake to inherently disclose loading a second array of key parameters into memory" is ***incorrect*** speculation. The value v represents the input pixel. For one set of control parameters (I_k, g_k, c_k), the corresponding values c_g for different values of v are loaded into the look up table. One value of c_g is generated for one input pixel value v sequentially.

It is understood that a traditional look up table (LUT) is very different from "a vector look up unit adapted to look up ***a vector of data items*** simultaneously". The description of Lake shows no ***vector*** look up unit. However, for example, claims 31 and 36 recite:

31. (original) A processing system to blend two images, the system comprising:
a vector register file comprising a plurality of vector registers;
a vector processing unit coupled to the vector register file, the vector processing unit comprising a vector look up unit adapted to look up a vector of data items simultaneously, the vector processing unit:
loading a vector of keys into a vector register in the vector register file;
converting the vector of keys into a first vector of blending factors for a first image and a second vector of blending factors for a second image using a plurality of look up tables in the vector look up unit; and
computing an image attribute for a blended image using the blending factors.

36. (original) A processing system to blend two images, the system comprising:
a vector register file comprising a plurality of vector registers;
a vector processing unit coupled to the vector register file, the vector processing unit comprising a vector look up unit adapted to look up a vector of data items simultaneously, the vector processing unit:
loading a first vector of keys into a vector register in the vector register file;

loading a second vector of keys into a vector register in the vector register file;

converting the first vector of keys into a first vector of blending factors for a first image and the second vector of keys into a second vector of blending factors for a second image using a plurality of look up tables in the vector look up unit; and

computing an image attribute for a blended image using the blending factors.

Thus, at least for the above reason, claims 31 and 36 are patentable over Takahashi in view of Lake.

Further, the examiner bears the initial burden of ***factually supporting*** any *prima facie* conclusion of obviousness under 35 U.S.C. 103. A *prima facie* case of obviousness is established by presenting *evidence* that would have led one of ordinary skill in the art to combine the relevant teachings of the references to arrive at the claimed invention. *It is impermissible to simply make a hindsight reconstruction of the claimed invention using the claim as a template and filling the gaps using the elements from the references.*

"The tendency to resort to hindsight upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." (MPEP 2142).

MPEP (2141) shows that "When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (A) The claimed invention must be considered as a whole; (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) Reasonable expectation of success is the standard with which obviousness is determined."

Further, MPEP (2142, 2143) shows that "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure."

A broad conclusory statement regarding the obviousness of modifying a reference, standing along, is not "evidence".

Lake shows "The FIG. 2 circuit includes only a single mixer (the circuitry identified by reference numeral 31)" (see, Column 5, lines 1-2, Lake) and "FIG. 2 circuit can perform this operation in a more efficient, less costly manner, employing fewer circuit components" (see, Column 5, lines 10-12, Lake). There is no a ***vector*** processing unit in Lake. Neither Lake nor Takahashi suggests vector processing.

Further, the Office Action asserted

> "One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the single LUT implementation of Lake ..." (Page 3, lines 20-12, Office Action mailed July 21, 2004).

which is a clear indication that the examiner failed to see any motivation to use multiple LUT tables in the context of Lake and Takahashi. Such a clear indication of motivation to modify clearly contradicts the conclusion of obviousness.

Thus, the suggested modifications to Lake and Takahashi are not motivated by the prior art references but based on the teaching of the present application. To make a *prima*

facie case of obviousness, the motivation or suggestion must be found in the cited references, not in the teaching of the present application. *Impermissible hindsight reconstruction* must be avoided.

The assertion of "the feature of having multiple LUT tables instead of a single LUT performing similar functions is matter of design choice as preferred by the designer and to which best suits the application at hand" is merely a broad conclusory statement. The Office Action shows no evidence to support the assertion of design choice.

Further, "to improve the efficiency and reduce costs of hardware involving in conventional video combining circuitry (see column 3, lines 49-61 of Lake)" is clearly inadequate as a motivation to combine Takahashi and Lake in a way suggested in the Office Action. Lake provides the circuit of Figure 2 to "perform this operation in a more efficient, less costly manner, employing fewer circuit components" (see column 5, lines 10-12, Lake). The circuit of Figure 2 of Lake uses only a single mixer and the similar look up table that has different contents (e.g., using a c_g look up table instead of a conventional α look up table). It is not evident how the combination of Takahashi and Lake in a way suggested in the Office Action actually improves the efficiency and reduces costs of hardware with respect to the individual circuits of Takahashi and Lake, which are completely different.

In fact, the description of Lake to have a single mixer and to reduce the number of components teaches away from the assertion of a design choice to add more LUT tables for no apparent benefits.

In summary, Takahashi and Lake do not teach each and every aspect of claims 31 and 36. Further, the motivations to make the modifications in a way shown in the Office Action are not based on the prior art references. Claims 32 and 37 are patentable over Takahashi and Lake at least for the reasons stated above, since they are dependent claims of claims 31

and 36. Thus, at least for the above reasons, withdrawal of the rejections under 35 U.S.C. 103(a) is respectfully requested.

Please charge any shortages or credit any overages to Deposit Account No. 02-2666. Furthermore, if an extension is required, Applicant hereby requests such extension.

Respectfully submitted,

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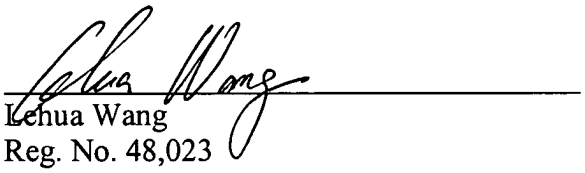

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